COMPARISON OF PMOS TRANSISTOR SOURCE/DRAIN DOPING: ION IMPLANTATION VERSUS SOLID DIFFUSION SOURCE

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ABSTRACT

This project was an investigation into transistor development in areas of implanted wells and source/drain regions. Wafer processing was put through the existing RIT PMOS process, but incorporated two areas of comparison: ion implantation of an n-type well, versus the use of an n-type substrate; and doping the p-type source/drain regions by implantation, versus solid diffusion sources. Experimental results for sheet resistance and junction depth were within ten percent of those predicted by SUPREM. Electrical testing results yielded no functional transistors. Diagnostics using diffused and implanted resistors in the wells indicated that the wells were too shallow to properly isolate these devices fabricated with this process.

INTRODUCTION

Complimentary Metal Oxide Semiconductor Technology (CMOS) incorporates n-channel and p-channel field effect devices on the same wafer. One or both of these devices is fabricated in a well or tub of opposite doping than the substrate for electrical isolation, as shown in Figure 1.

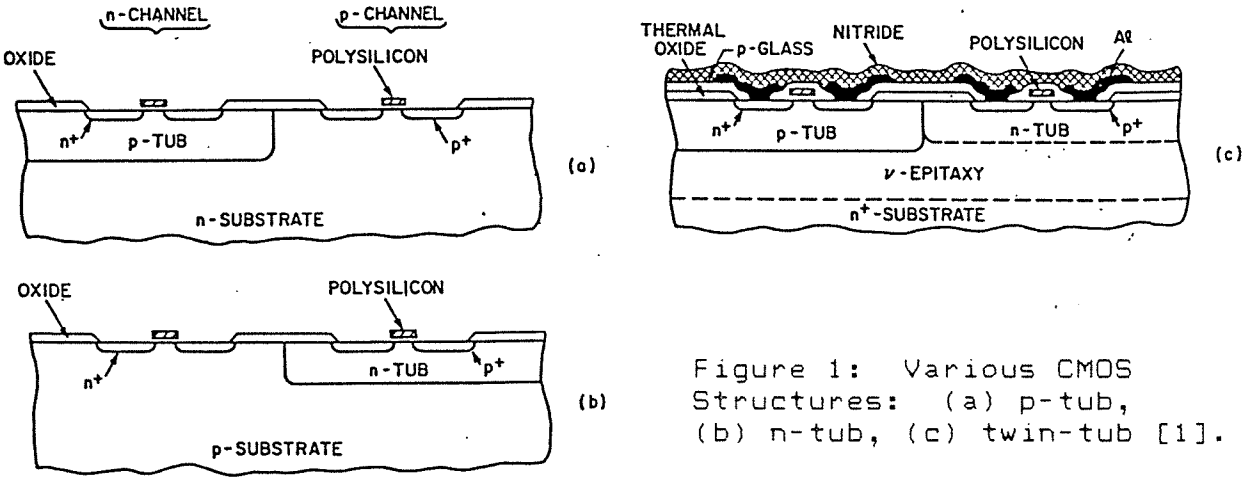


Figure 1: Various CMOS Structures: (a) p-tub, (b) n-tub, (c) twin-tub [1].

These wells are fabricated via ion implantation, because implantation offers advantages such as accurately controlled dose, minimal lateral diffusion, and a pure source of dopant atoms. In addition, implantation can take place through a thin oxide to prevent damage to the silicon surface, and the masking material does not need to withstand high temperatures. However, an anneal is required at a temperature above 950C to fully activate the lattice to remove the damage caused by the implant. Unless an anneal is performed after the implant, the electrical properties such as mobility and carrier lifetimes are degraded, due to the displacement of silicon atoms. Reference 2 contains an extensive discussion of ion implantation.

Well formation involves implanting dopant into a substrate at a concentration high enough to compensate the substrate in order to give good device characteristics and profiles with the desired doping. The doping is typically two to five times higher than that of the substrate to ensure this control [1].

Traditionally, p- or n-well structures make use of a deep impurity diffusion (drive-in) to form the well's depth. Since impurity atoms diffuse vertically and laterally, significant lateral area is lost, resulting in a lower packing density. References 3 and 4 provide a thorough discussion of the details listed above. Today with higher energy machines that can implant impurities to a deeper depth, this drive-in may be reduced. Since the annealing temperature doesn't need to be as high as a diffusion temperature, the implanted profiles show a smaller lateral spread. The resulting profile yields many improvements such as high conductivity and a low ohmic drop, improved punch-though voltage, reduced junction capacitance and body effect, and better latch-up immunity [5].

CMOS process development is underway at RIT to expand present fabrication capabilities. Currently, PMOS and bipolar processes exist which yield functioning transistors and small circuits. This project was an investigation into transistor development in areas of implanted wells and source/drain regions. Wafer processing was put through the existing RIT PMOS process, but incorporated two areas of comparison: ion implantation of an n-type well into a p-type wafer, versus that of no well and use of an n-type substrate; and secondly to dope the p-type source/drain regions by implantation, versus the use of solid diffusion sources. Figure 2 displays the transistor cross-sections of the four different processing cases just described.

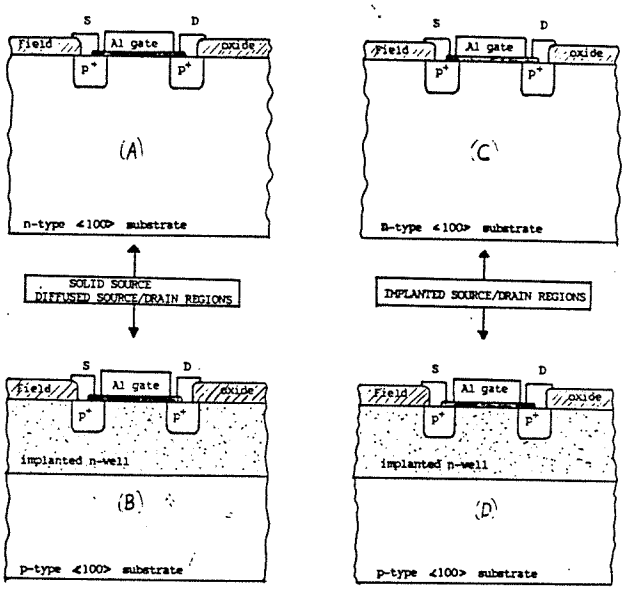


Figure 2:
(A): p-type Solid Source S/D into n-Substrate (No Well)

(B): p-type Solid Source S/D into n-type Implanted Well

(C): p-type Implanted S/D into n-Substrate (No Well)

(D): p-type Implanted S/D into n-type Implanted Well

EXPERIMENT

The final goal was to produce a comparable transistor family of I-V curves and threshold voltages between the 4 devices with the different processing backgrounds. Even with the different processing backgrounds, each product wafer was processed to obtain similar measured characteristics such as impurity concentrations, oxide thicknesses, sheet resistances, and junction depths. To obtain these similarities, matching of the solid diffusion source and implant data was achieved through the use of SUPREM II simulations and trial runs using control wafers.

The developed RIT PMOS process fabricated transistors with a metal (Aluminum) gate on a thin oxide, with diffused p-type source/drain regions into an n-type substrate. A brief outline of the fabrication process is shown in Figure 3 along with the wafer splits for the implanted well and source/drain regions. The process started with seven n-type, 5 to 8 ohm-cm, and seven p-type, 14-22 ohm-cm wafers. Both wafer types had <100> silicon orientation. Two n-type and two p-type wafers were considered as product while the other 10 wafers were used as controls. The controls were used for trial runs and in measurement of junction depth (Xj) by the Groove and Stain method, sheet resistance (RHOS) by the Four Point Probe, and oxide thickness (Tox) by a Nanospec instrument.

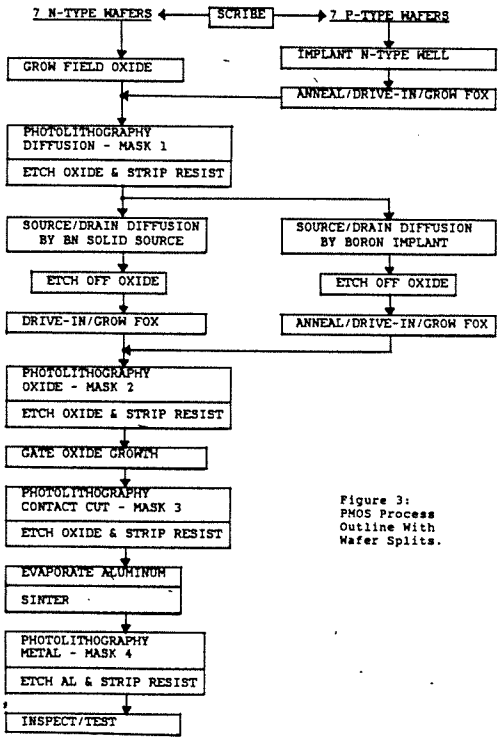


Figure 3:
PMOS Process Outline With Wafer Splits.

The n-type well was fabricated by implanting P+ phosphorus at a dose of 1E12 atoms/cm2 at an energy of 100keV, followed by a 1150C, 14 hour drive-in in dry oxygen. This was to produce an n-well of 4.0um in junction depth, 6.0 ohms-cm of resistivity, and a background concentration of 2e15 cm-3. These parameters correlated to the characteristics of the n-type wafer substrate. The source/drain regions were fabricated by implanting Boron 11 at a dose of 3E15 atoms/cm2 at an energy of 50keV, followed by 1050C, 90 minute drive-in. This was to produce source/drain regions of 1.8um in junction depth and 80 ohms/sq. of sheet resistance. These parameters correlated to the characteristics of the Carborundum BN-975 Planar Solid Diffusion Sources using the Hydrogen Injection process followed by a 1050C, 45 minute drive-in. Both implants were done through 500 Angstroms of a thin oxide. All the photolithography was performed with KTI820 positive resist, exposed on Kasper contact aligners, and developed with a 1:1 mix of ZX934 developer to D.I. water. A complete process outline is contained in Appendix 1.

This process used the four standard RIT PMOS photolithography mask set having layer names of diffusion, oxide, contact cut, and metal. The mask set incorporated test cells for PMOS, bipolar, and NMOS devices having ten micron design rules. Four of the twenty cells contained in one die of the mask set can be seen in Appendix 2. These four cells contained p-diffused resistors in cell 2, four different sized PMOS transistors in cell 4, and a few PMOS logic circuits in cells 5 and 6.

RESULTS/DISCUSSION

Table 1 summarizes the experimental junction depth and sheet resistance processing characteristics as compared to SUPREM II simulations. Many of the cases were within ten percent. Final SUPREM profiles for the four different processing cases can be seen in Appendix 3. The Solid Source diffused p-type source/drain had a higher sheet resistance than the implanted source/drain. This could have been lowered with a shorter drive-in and less oxidation. The wafers with the implanted n-well had deeper source/drain junction depths than those with the n-substrate.

COMPARISON OF SUPREM TO LABORATORY RESULTS

POST N-WELL DRIVE-IN RESULTS:

#	JUNCTION DEPTH (Xj) SUPREM	Actual	% Diff	SHEET RESISTANCE (RHOS) SUPREM	Actual	% Diff
B/D :	4.15	3.87	7.2	10357	6029	71.8

POST SOURCE/DRAIN DRIVE-IN RESULTS:

#	JUNCTION DEPTH (Xj) SUPREM	Actual	% Diff	SHEET RESISTANCE (RHOS) SUPREM	Actual	% Diff
A :	1.83	1.71	7.0	116.8	106.0	10.2
B :	1.80/4.03	1.85/3.34	2.7/20.7	112.9	106.5	6.0
C :	1.69	1.67	1.2	70.8	68.8	2.9
D :	1.64/4.00	1.91/3.82	14.1/4.7	70.8	71.4	0.8

POST GATE OXIDE GROWTH RESULTS:

#	JUNCTION DEPTH (Xj) SUPREM	Actual	% Diff	SHEET RESISTANCE (RHOS) SUPREM	Actual	% Diff
A :	1.86	1.72	8.1	121.7	111.9	8.8
B :	1.84/4.00	1.90/3.57	3.2/12.0	117.6	108.7	8.2
C :	1.70	1.76	3.4	75.0	73.5	2.0
D :	1.65/3.97	1.98/3.61	16.7/9.9	75.0	76.2	1.6

KEY: A : p-type Solid Source S/D into n-Substrate (No Well).
B : p-type Solid Source S/D into n-type Implanted Well.
C : p-type Implanted S/D into n-Substrate (No Well).
D : p-type Implanted S/D into n-type Implanted Well.

TABLE 1 - FIGURE 4

The testing results proved differently. The transistors did not function properly and produced I-V characteristic much like diodes. In addition they were very susceptible to light and substrate grounding effects. So the focus was shifted toward the resistors to get some working devices and attempt to figure out why the transistors were not working.

The uniformity across the wafer for two different length p-type resistors was displayed in Table 2. Only three of the four wafers were displayed in table 2 because the standard PMOS process wafer was broken during processing. The Resistance (R) was measured from the slope of the I-V curves. The sheet resistance was calculated from the resistance and the W/L ratio, but the contact resistance was not taken into account. The obvious effect of this assumption was that sheet resistance extracted from resistors A and B were not equal. However, it was seen that the resistors placed in the substrate exhibited a larger range of values. Further conclusions were not drawn because the standard PMOS wafer was broken.

RESULTS OF RESISTOR UNIFORMITY ACROSS THE WAFER

(B) p-type Solid Source Diffused Resistor into an n-type Well

	RESISTOR A (L/W=1740/10 um)		RESISTOR B (L/W=860/10 um)	
Pos.	R (Kohm)	RHOS (ohm/sq)	R (Kohm)	RHOS (ohm/sq)
T	20.3	116.7	10.5	122.1
C	20.6	118.4	10.6	123.2
B	21.2	121.8	11.0	127.9
L	20.4	117.2	10.7	124.4
R	20.7	119.0	10.6	123.2
AVE.	20.6	118.6	10.7	124.2
ST.DEV	0.3	1.8	0.2	2.0
4 PT PROBE	--	108.7	--	108.7
% Diff	--	8.3	--	12.5

(C) p-type Implanted Resistor into n-Substrate (No Well).

	RESISTOR A (L/W=1740/10 um)		RESISTOR B (L/W=860/10 um)	
Pos.	R (Kohm)	RHOS (ohm/sq)	R (Kohm)	RHOS (ohm/sq)
T	14.7	84.5	7.43	86.4
C	15.7	90.2	7.89	91.7
B	15.5	89.1	8.09	94.1
L	14.4	82.7	7.62	88.6
R	15.9	91.4	8.12	94.4
AVE.	15.2	87.6	7.83	91.0
ST.DEV	0.6	3.4	0.3	3.1
4 PT PROBE	--	73.5	--	73.5
% Diff	--	16.1	--	19.2

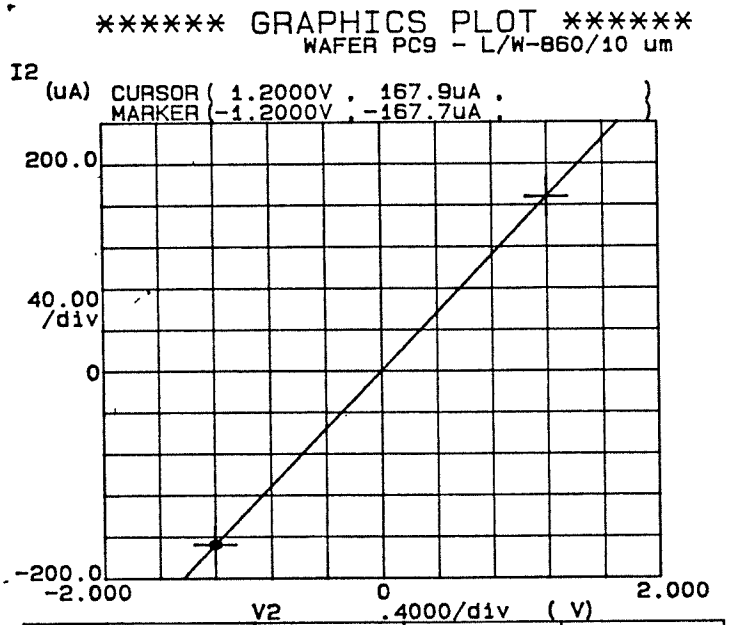
(D) p-type Implanted Resistor into n-type Implanted Well.

	RESISTOR A (L/W=1740/10 um)		RESISTOR B (L/W=860/10 um)	
Pos.	R (Kohm)	RHOS (ohm/sq)	R (Kohm)	RHOS (ohm/sq)
T	13.7	78.7	7.14	83.0
C	13.6	78.2	7.15	83.1
B	13.9	79.9	7.23	84.1
L	13.7	78.7	7.09	82.4
R	14.2	81.6	7.39	85.9
AVE.	13.8	79.4	7.20	83.7
ST.DEV	0.2	1.2	0.1	1.2
4 PT PROBE	--	76.2	--	76.2
% Diff	--	4.0	--	8.9

TABLE 2 - FIGURE 5

These results were somewhat misleading, because the I-V characteristics for all the resistors were not linear except in the -2.0 to 2.0 volt region. As the voltage was increased the I-V curve became nonlinear as shown in Figures 6 and 7. The lines numbered 1 through 4 were the effects of light, and grounding of the substrate, on the same resistor. The slope of the I-V curve increased from a non-lighted and non-grounded substrate (line 1), to a lighted and grounded substrate (line 4). These same characteristics were seen for the transistors. At higher currents the shallow n-well breaks down to form two parallel resistors, producing the steeper slopes. One resistor would be the actual surface p-type resistor, while the other would be a parasitic resistor in the p-type substrate. In addition, with only a 1.5 to 2 micron distance between the bottom of the p-type diffusion and the top of the p-type substrate, the thin n-well forms a parasitic PNP transistor when grounded. So in this situation, the n-well acts as the transistor base region,

and when light is projected onto the wafer, the base becomes more energetic to produce a steeper slope.

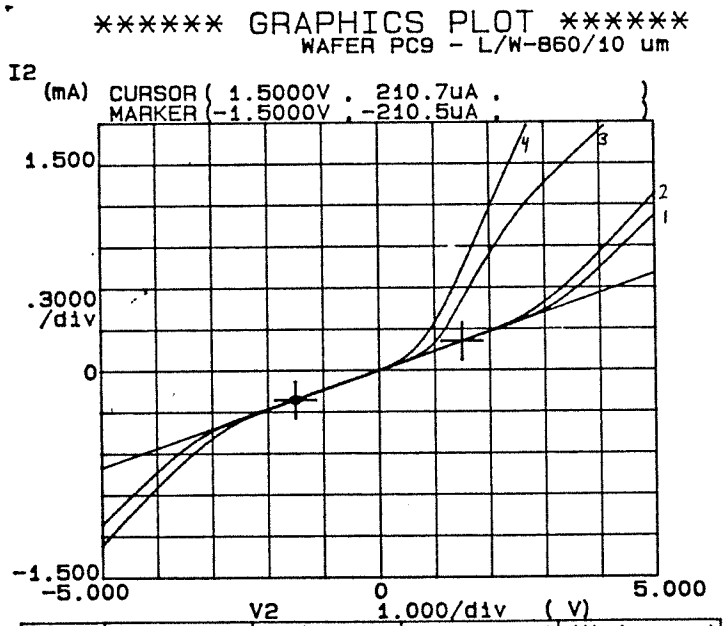


Variable1:
V2 -Ch2
Linear sweep
Start -2.0000V
Stop 2.0000V
Step .0400V

Constants:
Vi -Chi .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	140E-06	7.15E+03	-880E-06	123E-09
LINE2				

Figure 6



Variable1:
V2 -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .1000V

Constants:
Vi -Chi .0000V
V8 -Ch3 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	140E-06	7.12E+03	-531E-06	74.5E-09
LINE2				

Figure 7:
1: Not Lighted & not grounded
2: Lighted & not grounded
3: Not Lighted & grounded
4: Lighted & grounded

CONCLUSION

Many of the junction depth and sheet resistance experimental results were within ten percent of those predicted by SUPREM simulations.

The testing results proved differently. The transistors did not function properly and produced I-V characteristic much like diodes, but were very susceptible to light and substrate grounding effects, due to the shallow n-well with only 1.5 to 2 micron distance between the bottom of the p-type diffusion and the top of the p-type substrate. So the focus was shifted toward the resistors. The resistors showed very good uniformity but only for a narrow -2 to 2 volt window. For higher voltage ranges, substrate grounding and lighting effects produced nonlinear tails on the curves. These effects were caused by parasitic substrate resistor and parasitic transistor formation, once again due to the shallowness of the n-type well.

So the advantages of p-type source/drain implantation over Solid Diffusion Sources, and an implanted n-type well over an n-type substrate, still remains open for future investigation and improvement with these poor results. Some recommendations for the project's improvement would involve a deeper well on the scale of 5 to 6 microns in depth, shallower p-diffused regions of less than one micron, and beginning with a p-type substrate with lower background resistivity on the order of 1 to 5 ohm-cm.

ACKNOWLEDGMENTS

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